Scalability Revisited: 100 nm PD-SOI Transistors and Implications for 50 nm Devices

K. Mistry, T. Ghani, M. Armstrong, S. Tyagi, P. Packan*, S. Thompson, S. Yu*, M. Bohr
Portland Technology Development, *TCAD, Intel Corp. Hillsboro, OR, USA

Abstract

We describe 100nm gate length PD-SOI transistors with the best SOI I_{on}-I_{off} characteristics reported for the 0.18μm technology generation. SOI inverter delay is 7.4 ps at Vdd=1.5V and L_{gate}=100 nm. Inverter delays show 16% (fanout=1) and 8% (fanout=4) improvement over comparable bulk CMOS. Scaling analysis for PD-SOI shows a reduced role for junction capacitance and an increased history effect for scaled devices, so that SOI has significantly diminished performance gain relative to bulk CMOS for 50nm devices (0.1μm generation).

Introduction

Partially Depleted SOI (PD-SOI) transistors have been shown to have performance improvement over bulk CMOS for 0.25um technologies, but the scalability of this performance gain to more aggressive technologies has been debated [1,2]. In this work, we evaluate the performance benefit of 100nm PD-SOI transistors suitable for the 0.18 μm technology node and then evaluate the scalability of this performance gain to 50 nm devices (0.1 μm generation).

100nm Transistor Performance

SOI and bulk transistors (see Table I) are fabricated with the process in [3]. SIMOX SOI wafers have final silicon layer and buried oxide thickness of 190 nm. Figs 1 & 2 show threshold voltage and transistor off current vs. L_{gate} for NMOS SOI and bulk devices. After optimizing floating body DIBL using lifetime adjust implantation [4], linear V_{th} for SOI NMOS devices needs to be set 40-50 mV higher to achieve similar I_{off}=5 nA/μm and similar saturated V_{th} as bulk devices at L_{gate}=100 nm. PMOS SOI devices at L_{gate}=110 nm (Figs. 1 & 3) require 30 mV higher linear V_{th} to achieve matched I_{off}=30 nA/μm.

Fig. 4 and 5 show bulk and SOI I_{dsat} vs. I_{off}. NMOS devices at I_{off}=5 nA/μm show I_{dsat}=1000 μA/μm for bulk vs. 910 μA/μm for SOI; of this 9% reduction for SOI, 6-7% is due to self-heating, while 2-3% is due to the higher V_{th}. PMOS devices at I_{off}=30 nA/μm show 490 μA/μm for both bulk and SOI. The SOI I_{on}-I_{off} characteristics are significantly better (10-15% higher I_{on}) than previously reported for 0.18 μm technology generation transistors [5]. Fig. 6 shows SOI transistor I_d-V_d characteristics. The dashed curve shows SOI pulsed I-V with 6-7% higher I_{dsat}.

Ring oscillator measurements comparing SOI and bulk were obtained using transistors identical to those described above except that NMOS I_{off} was 3X higher for SOI than for bulk NMOS at L_{gate} of 100-110 nm. Figs. 7 & 8 show inverter delay per stage vs. L_{gate} at Vdd=1.5V for fanout=1 & 4. Fanout=1 inverter delay at L_{gate}=100 nm is 7.4 ps for SOI and 9 ps for bulk. Fanout=4 inverter delay is 39.5 ps for SOI and 44 ps for bulk. Drive currents and inverter delays are expected to improve 5-10% with the process improvements described in [6].

SOI delay improvement relative to bulk is 18% and 10% for fanout of 1 and 4, reducing to 16% and 8% respectively after accounting for the 3X off current difference between SOI and bulk NMOS devices. SOI benefit for fanout=1 gate delay is significantly less than the 25% previously reported [2] due to aggressive reduction of junction capacitance for our bulk CMOS.

TABLE I
Summary of Key Transistor Features
*SOI Idsat not corrected for self-heating

	SOI		Bulk	
	NMOS	PMOS	NMOS	PMOS
Vdd (V)	1.5	1.5	1.5	1.5
Lg (nm)	100	110	100	110
Tox (nm)	3	3	3	3
Vt (lin) (mV)	460	350	420	320
Vt (sat) (mV)	270	140	280	140
Idsat* (μA/μm)	910	490	1000	490
Ioff (nA/μm)	5	30	5	30

Technology Scaling Trends for PD-SOI

Next we evaluate the scalability of SOI performance gain to 50 nm devices (0.1 μm technology). The relative benefit of SOI will reduce because the impact of junction capacitance diminishes with scaling. Fig. 9 shows the scaling trend for percent junction capacitance loading for fanout=1 & 4. For fanout=1, this load diminishes from 10% for 0.18μm technology to 5% for 0.1μm technology. Junction area capacitance loading decreases as the square of the scale factor while gate and perimeter capacitances decrease only linearly. For larger fanout, the loading due to junction capacitance is even smaller.

Another SOI parameter that scales poorly is the history effect on delay. Fig 10 shows the percent variation in SOI delay due to switching history from [7] & [2]. History effect for our devices is substantially similar. Delay uncertainty due to history increases from 5-6% for 0.18μm technology to 7-8% for 0.1μm.

Fig. 11 shows the expected SOI performance gain vs. bulk for fanout=1, with error bars representing the history effect uncertainty of SOI delay. Average delay improvement reduces from 16% for 0.18μm technology to 11% for 0.1 μm technology, while the worst case delay improvement drops from 13% to 7%. For fanout=4 (Fig. 12), the average improvement drops from 8% for 0.18μm to 6% for 0.10μm, while the worst case drops from 5% to 2%. For 50 nm devices, the performance gain from SOI diminishes dramatically. Because product performance is increasingly affected by interconnect delays, the net benefit of SOI would be even smaller.

Conclusions

100 nm devices described have the best I_{on}-I_{off} characteristics reported for 0.18 μm generation PD-SOI. SOI inverter delay of 7.4 ps is obtained at Vdd=1.5V and L_{gate}=100 nm. However, the expected performance gain for PD-SOI diminishes dramatically for 50nm devices due to (i) aggressive reduction of junction capacitance for our bulk CMOS, (ii) the reduced impact of area junction capacitance with scaling, and (iii) increased history effect on delay for scaled Vdd.

References

[1] R. Chau et al., *IEDM Tech. Digest*, pp. 591-594, 1997.
[2] E. Leobandung et al., *IEDM Tech. Digest*, pp. 403-406, 1998.
[3] S. Yang et al., *IEDM Tech. Digest*, pp. 197-200, 1998.
[4] K. Mistry et al., *IEEE Trans. Elect. Dev.*,p. 2201, Nov. 1999.
[5] E. Leobandung et al., *IEDM Tech. Digest*, pp. 679-682, 1999
[6] T. Ghani et al., *IEDM Tech. Digest*, pp. 415-419, 1999.
[7] F. Assaderaghi et al., *Symp. VLSI Tech. Dig.*, p. 122, 1996.

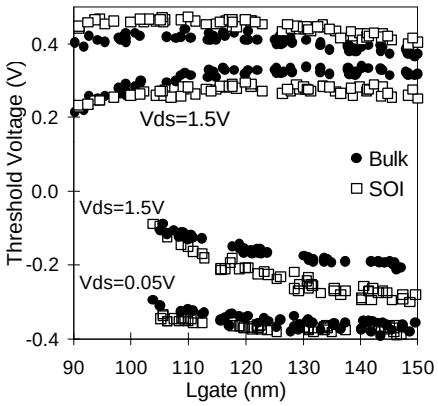


Fig. 1 Linear and saturated V_{th} vs. gate

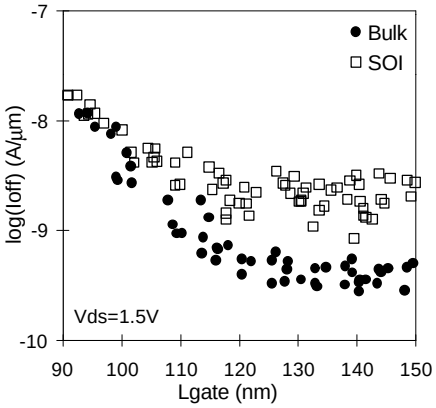


Fig. 2 NMOS off current vs. gate length

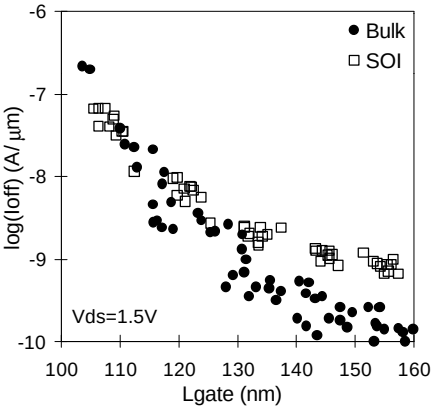


Fig. 3 PMOS off current vs. gate length.

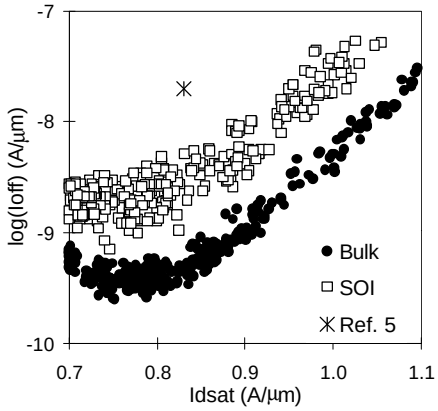


Fig. 4 NMOS drive current vs. off current. (SOI not corrected for self-heating)

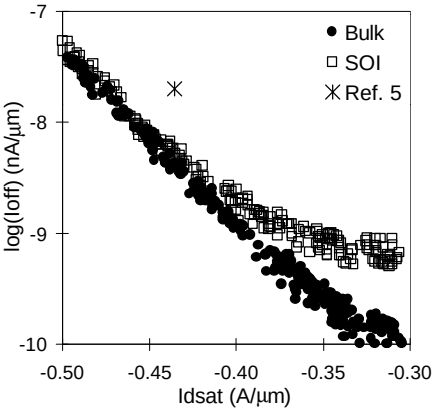


Fig. 5 PMOS drive current vs. off current

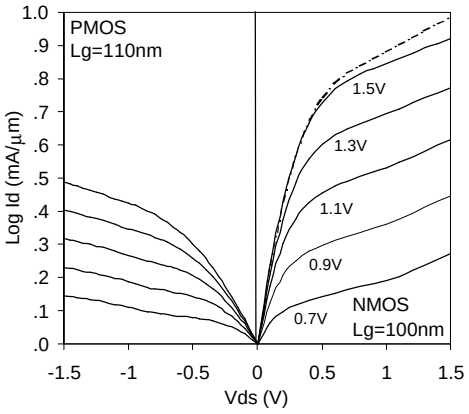


Fig. 6 SOI NMOS & PMOS I_d-V_d curves. Dashed curve is pulsed I-V with no self-heat.

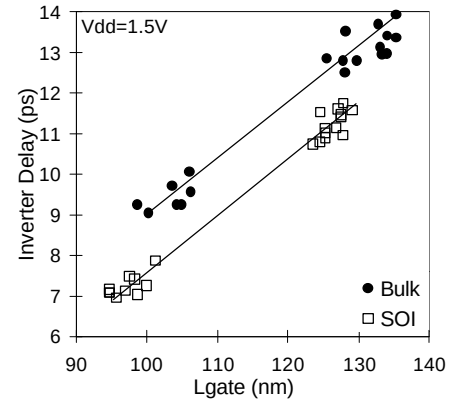


Fig. 7 Ring oscillator delay. for fanout=1

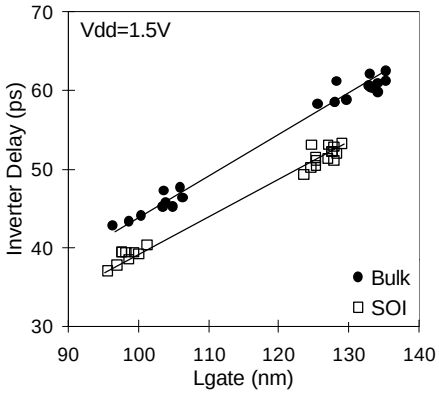


Fig. 8 Ring oscillator delay for fanout=4

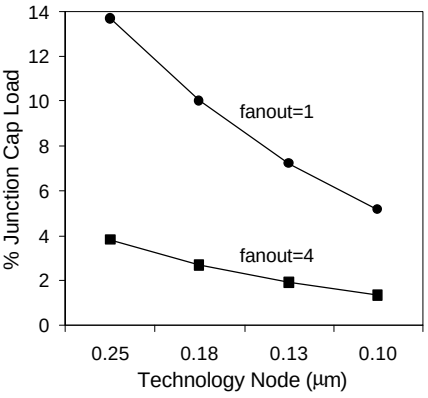


Fig. 9 Junction cap. loading vs. technology

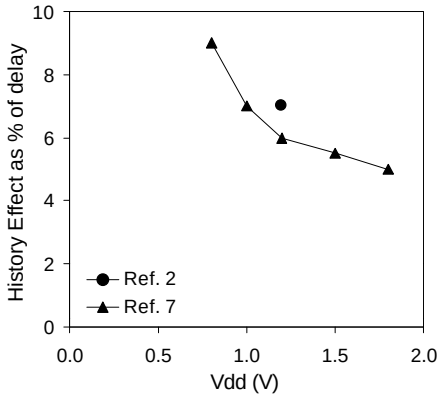
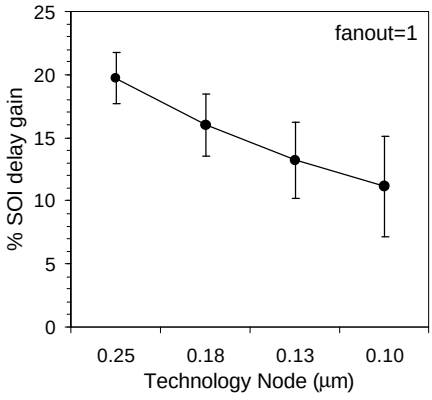
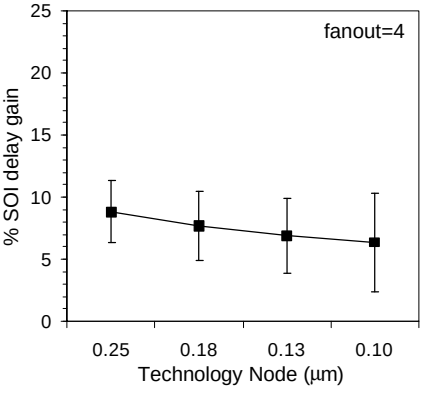


Fig. 10 History Effect vs. Vdd from Ref. 2,7.





Figs. 11 & 12 SOI vs. bulk performance scaling trends. Error bars represent history effect.